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10/651,324	08/28/2003	Christopher K. Morzano	MCT.0047C1US (99.0404.1)	7800

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EXAMINER

CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/651,324

Applicant(s)

CHRISTOPHER K. MORZANO

Examiner

Mardochee Chery

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 37-71 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 37-71 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to Application No. 10/651324 filed on August 28, 2003.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claim 1 rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 6,615,331. This is a double patenting rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 37, 42-43, 46, 52, 57-58, 61, 65, and 67 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the

inventor(s), at the time the application was filed, had possession of the claimed invention. Although "Column redundancy check" is mentioned in the specification, applicant fails to describe procedures on how to perform and carry out such process.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1 and 37-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy (6,125,421) in view of Hsu et al. (5,889,727).

As per claim 1, Roy discloses a method usable with a memory device, comprising receiving a data strobe signal from a memory bus [*data has been received by the read data buffer unit 73; col.19, lines 22-23*]; capturing data associated with a write command from the memory bus in synchronization with the data strobe signal [*a synchronous mode in which at least two of the multi-line channels are synchronized together to provide data associated with a particular read and/or write transaction to two or more clusters simultaneously; col.7, lines 33-37*]; and synchronizing the beginning of an internal write operation to a

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memory cell array of the memory device to a clock signal [*synchronization for data transfer (read and/or write)) in both directions; under this clock synchronization technique, the clock signal follows slightly after the data transferred across the interface in either direction; col.12, lines 26-29; it is possible to have the memory cell data associated with different row/column addresses latched into the different banks; col.12, lines 10-12*].

However, Roy does not specifically teach performing a column redundancy check in response to an address associated with the write command as recited in the claim.

Hsu et al. discloses performing a column redundancy check in response to an address associated with the write command [*the column redundancy check 104 enables a normal column path enable signal; a redundancy selector to enable a read/write operation; col.1, lines 47-54*] to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51).

Since the technology for reducing cycle time using column redundancy check was well known as evidenced by Hsu et al. and since performing column redundancy check indicates that a normal memory cell is accessed and a column redundant cell is used, an artisan would have been motivated to implement this feature in the system of Roy. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Roy to include column redundancy check since it was well known to indicate that a normal memory cell is

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accessed and a column redundant cell is used (col.1, lines 48-51) as taught by Hsu et al..

As per claim 37, Roy discloses a method usable with a memory device, comprising performing a column redundancy check []; and synchronizing the beginning of an internal write operation to a memory cell array of the memory device to a clock signal [*synchronization for data transfer (read and/or write)) in both directions; under this clock synchronization technique, the clock signal follows slightly after the data transferred across the interface in either direction; col.12, lines 26-29; it is possible to have the memory cell data associated with different row/column addresses latched into the different banks; col.12, lines 10-12*].

However, Roy does not specifically teach performing a column redundancy check as recited in the claim.

Hsu et al. discloses performing a column redundancy check [*the column redundancy check 104 enables a normal column path enable signal; col.1, lines 47-50*] to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51).

Since the technology for reducing cycle time using column redundancy check was well known as evidenced by Hsu et al. and since performing column redundancy check indicates that a normal memory cell is accessed and a column redundant cell is

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used, an artisan would have been motivated to implement this feature in the system of Roy. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Roy to include column redundancy check since it was well known to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51) as taught by Hsu et al..

As per claim 43, Roy discloses a method usable with a memory device, comprising providing column select signals indicative of a column address to a memory cell array of the memory device [*column select circuitry that transfers the first column address to the memory device; col.16, lines 30-35; it is possible to have the memory cell data associated with different row/column addresses latched into the different banks; col.12, lines 10-12*].

However, Roy does not specifically teach performing a column redundancy check prior to the initiation of the providing of the column select signals as recited in the claim.

Hsu et al. discloses performing a column redundancy check prior to the initiation of the providing of the column select signals [*the column redundancy check 104 enables a normal column path enable signal; a redundancy selector to enable a read/write operation; col.1, lines 47-54; the local CF generator generates a redundancy bit-line selector; the redundancy evaluation will not be performed until the global factors arrive at the column redundancy check; col.1, lines 52-57*] to

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indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51).

Since the technology for reducing cycle time by performing a column redundancy check prior to the initiation of the providing of the column select signals was well known as evidenced by Hsu et al. and since performing a column redundancy check prior to the initiation of the providing of the column select signals indicates that a normal memory cell is accessed and a column redundant cell is used, an artisan would have been motivated to implement this feature in the system of Roy. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Roy to include performing a column redundancy check prior to the initiation of the providing of the column select signals since it was well known to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51) as taught by Hsu et al..

As per claim 52, Roy discloses a memory device comprising a memory cell array [*memory location within the array, including the same memory cell*; col.6, lines 21-22]; a first circuit to perform a column redundancy check in response to a decoded address [*the column address information is decoded within the column control logic unit 37*; col.26, lines 20-25]; a second circuit to synchronize an initiation of an internal write operation to the memory cell array with a clock signal [*transfer the newly written data back to the memory cell; the timing relationship between the write data and the column select signals may be the same as for a column burst*

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write transaction; col.36, lines 8-11; synchronization for data transfer (read and/or write)) in both directions; under this clock synchronization technique, the clock signal follows slightly after the data transferred across the interface in either direction; col.12, lines 26-29].

However, Roy does not specifically teach performing a column redundancy check as recited in the claim.

Hsu et al. discloses performing a column redundancy check [*the column redundancy check 104 enables a normal column path enable signal; a redundancy selector to enable a read/write operation; col.1, lines 47-54; the local CF generator generates a redundancy bit-line selector; the redundancy evaluation will not be performed until the global factors arrive at the column redundancy check; col.1, lines 52-57]* to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51).

Since the technology for reducing cycle time by performing a column redundancy check was well known as evidenced by Hsu et al. and since performing a column redundancy check indicates that a normal memory cell is accessed and a column redundant cell is used, an artisan would have been motivated to implement this feature in the system of Roy. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Roy to include performing a column redundancy check because it was well known to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51) as taught by Hsu et al..

As per claim 58, Roy discloses a memory device comprising a memory cell array [memory location within the array, including the same memory cell; col.6, lines 21-22]; an addressing circuit [carry both address and data information for conducting selected read and/or write transactions; col.7, lines 14-17]; and a control circuit to cause the addressing circuit to perform a column redundancy check during a delay to accommodate variations in the timing of a data strobe signal and begin providing column select signals to the memory cell array after performing the column redundancy check [address and control information for a particular transaction; col.7, lines 29-31; data from each new random column address is provided delayed by the column address access time; col.28, lines 7-10; CLKIN pulses may be required following the last data byte in order to allow a delay in the write data path sufficient to match properly with the corresponding column select signals; col.35, lines 18-21; after memory cells have been read, column selection can be initiated; col.19, lines 60-62].

However, Roy does not specifically teach performing a column redundancy check as recited in the claim.

Hsu et al. discloses performing a column redundancy check [the column redundancy check 104 enables a normal column path enable signal; a redundancy selector to enable a read/write operation; col.1, lines 47-54; the local CF generator generates a redundancy bit-line selector; the redundancy evaluation will not be performed until the global factors arrive at the column redundancy check; col.1, lines 52-57] to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51).

Since the technology for reducing cycle time by performing a column redundancy check was well known as evidenced by Hsu et al. and since performing a column redundancy check indicates that a normal memory cell is accessed and a column redundant cell is used, an artisan would have been motivated to implement this feature in the system of Roy. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Roy to include performing a column redundancy check because it was well known to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51) as taught by Hsu et al..

As per claim 65, Roy discloses a computer system comprising a memory bus [*address bus*; col.1, line 26]; a memory controller coupled to the memory bus [*memory device and associated controller device*; col.8, lines 56-57]; a central processing unit to cause the memory controller to furnish signals to the memory bus to cause a memory operation [*controller logic units 12 that represent standard units associated with CPU or controller circuits*; col.10, lines 39-41]; and a memory device coupled to the memory bus and adapted establish a predetermined window of time to capture the data, and perform a column redundancy check in response to the memory operation during the predetermined window of time [*it may be necessary to hold the data bytes within a the input data buffer unit 178 for a period of time before sending the data for synchronization of the I/O write operations with the column select signal 181*; col.15, lines 61-66].

However, Roy does not specifically teach performing a column redundancy check as recited in the claim.

Hsu et al. discloses performing a column redundancy check [*the column redundancy check 104 enables a normal column path enable signal; a redundancy selector to enable a read/write operation; col.1, lines 47-54; the local CF generator generates a redundancy bit-line selector; the redundancy evaluation will not be performed until the global factors arrive at the column redundancy check; col.1, lines 52-57*] to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51).

Since the technology for reducing cycle time by performing a column redundancy check was well known as evidenced by Hsu et al. and since performing a column redundancy check indicates that a normal memory cell is accessed and a column redundant cell is used, an artisan would have been motivated to implement this feature in the system of Roy. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Roy to include performing a column redundancy check because it was well known to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51) as taught by Hsu et al..

As per claim 38, Roy discloses the internal write operation begins on an edge of the clock signal [*one byte would be transferred into the memory device on the rising edge of CLKIN; col.16, lines 23-25*].

As per claim 39, Roy discloses providing column select signals to the memory cell array in synchronization with the clock signal [*the column select circuitry using the same clock edge that transfers the first column of the burst, which is the falling edge; col.16, lines 30-33; it is possible to have the memory cell data associated with different row/column addresses latched into the different banks; col.12, lines 10-12*].

As per claim 40, Roy discloses the providing of the column select signals comprises latching the column select signals synchronously with an edge of the clock signal [*column address information is latched into the column address buffers within the column control logic unit 37; col.26, lines 5-8; the internal column select signal can be enabled; at that point there needs to be at least the same number of CLKIN pulse edges as the burst count; col.35, lines 26-29*].

As per claims 41 and 44, Roy discloses the latching of the column select signals comprises asserting a column address trap signal synchronously with the edge of the clock signal [*the column select circuitry uses the same clock edge that transfers the first column address of the burst; col.16, lines 30-33; separate clock pins to synchronize the data for each direction, although the same synchronization function could be achieved with a single clock pin; the transferred clock signal is used to latch in the data; col.14, lines 43-49; synchronization control unit 79, data latches 82; col.12, lines 46-48*].

As per claim 42, Roy discloses the column select signals begins on another edge of the clock signal [*the column select circuitry uses the same clock edge that transfers the first column address of the burst*; col.16, lines 30-33].

However, Roy does not specifically teach the column redundancy check is performed beginning on a first edge of the clock signal.

Hsu et al. discloses the column redundancy check is performed beginning on a first edge of the clock signal [*the column factors are directed to a column redundancy check 104 when a column synchronous pulse comes up the column redundancy check 104 enables a normal column signal*; col.1, lines 43-48] to indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51).

Since the technology for reducing cycle time by performing the column redundancy check on a first edge of the clock was well known as evidenced by Hsu et al. and since performing the column redundancy check on a first edge of the clock indicates that a normal memory cell is accessed and a column redundant cell is used, an artisan would have been motivated to implement this feature in the system of Roy. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant, to modify the system of Roy to include performing the column redundancy check on a first edge of the clock since it was well known to

indicate that a normal memory cell is accessed and a column redundant cell is used (col.1, lines 48-51) as taught by Hsu et al..

As per claim 45, the rejection of claim 41 above is herein incorporated. Roy further discloses latching data associated with a write command in response to a data strobe signal [*data associated with different row/column addresses latched into the different banks data that has been read or written*; col.12, lines 10-14].

As per claim 46, the rationale in the rejection of claim 42 above is herein incorporated.

As per claim 47, Roy discloses another edge comprises the next successive edge of the clock signal after the first edge [*a transfer made on the rising edge of CLKIN, and a second transfer made on the falling edge (next successive edge) of CLKIN*; col.16, lines 23-27].

As per claim 48, Roy discloses asserting another signal to equalize a data I/O line of the memory device for a first time interval that begins after the providing of the column select signals [*it may be necessary to hold the data bytes within a the input data buffer unit 178 for a period of time before sending the data for synchronization of the I/O write operations with the column select signal 181*; col.15, lines 61-66].

As per claim 49, Roy discloses deasserting another signal to terminate the first time interval *[it is possible to stop pulsing the CLKIN signal after the required number of pulses to support the pulse length have been sent; col.17, lines 16-19];* and beginning an internal read operation after the deassertion of said another signal *[a two-byte row/column burst read transaction is clocked into the memory device by two clock pulses of CLKIN, after which the CLKIN signal can stop until the internal row address sequence has progressed to where the internal column select address can be enabled; col.35, lines 21-26].*

As per claim 50, Roy discloses asserting said another signal after the beginning of an internal read operation for a second time interval less than the first time interval *[a two-byte row/column burst read transaction is clocked into the memory device by two clock pulses of CLKIN, after which the CLKIN signal can stop until the internal row address sequence has progressed to where the internal column select address can be enabled; col.35, lines 21-26; cycle time that is significantly less than their access time; col.2, lines 9-11].*

As per claim 51, Roy discloses the memory device comprises a double data rate (DDR) synchronous dynamic random access memory ISDRAM *[synchronous SRAMs have a cycle time that is significantly less than their access time; col.2, lines 9-11; a transfer made on the rising edge of CLKIN, and a second transfer made on the falling edge (next successive edge) of CLKIN; col.16, lines 23-27].*

As per claim 53, Roy discloses the second circuit synchronizes the initiation of an internal write operation to an edge of the clock signal [*synchronization for data transfer (read and/or write)) in both directions; under this clock synchronization technique, the clock signal follows slightly after the data transferred across the interface in either direction*; col.12, lines 26-29].

As per claim 54, Roy discloses the first circuit further provides column select signals to the memory cell array in synchronization with the clock signal [*operation initiated and controlled by control signals 85 from the control unit 77 to enable the write data buffer unit 78*; col.15, lines 16-19; *the CLKOUT signal is used primarily for the synchronization of the read data transmitted from the memory device*; col.15, lines 23-25].

As per claim 55, Roy discloses the first circuit latches the column select signals synchronously with an edge of the clock signal [*synchronization of the I/O write operations with the column select signal 181*; col.15, lines 64-66; *column select circuitry that transfers the first column address to the memory device*; col.16, lines 30-35; *it is possible to have the memory cell data associated with different row/column addresses latched into the different banks*; col.12, lines 10-12].

As per claim 56, Roy discloses the second circuit pulses a column address trap signal synchronously with an edge of the clock signal, and the first circuit latches the column select signals in response to a pulse of the column address trap signal [*an eight byte burst would require eight continuous clock edges (or five total clock pulses due to the initial rising edge)*; *it is possible to stop pulsing the CLKIN signal after the required number of pulses to support the burst length have been sent*; col.17, lines 13-18].

As per claim 57, the rationale in the rejection of claim 42 above is herein incorporated.

As per claim 59, Roy discloses the addressing circuit provides the column select signals by latching the column select signals synchronously with an edge of a clock signal [*it is possible to have the memory cell data associated with different row/column addresses latched into the different banks; col.12, lines 10-12; the internal column select signal can be enabled; there needs to be at least the same number of CLKIN pulse edges as the burst count; col.35, lines 26-29*].

As per claim 60, Roy discloses the addressing circuit latches the column select signals in response to a column address trap signal, and the control circuit asserts column address trap signal synchronously with the edge of the clock signal [*column address information is latched into the column address buffers within the column control logic unit 37; col.26, lines 5-8; the internal column select signal can be enabled; there needs to be at least the same number of CLKIN pulse edges as the burst count; col.35, lines 26-29*].

As per claim 61, the rationale in the rejection of claim 42 above is herein incorporated.

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As per claim 62, the rationale in the rejection of claim 47 above is herein incorporated.

As per claim 63, the rationale in the rejection of claim 48 above is herein incorporated.

As per claim 64, the rationale in the rejection of claim 51 above is herein incorporated.

As per claim 66, Roy discloses the signals include signals that indicate a write command, and the memory device is further adapted to capture said signals that indicate the write command in synchronization with a clock signal and begin an internal write operation to a memory cell array of the memory device in synchronization with the clock signal [*synchronization for data transfer (read and/or write)) in both directions; under this clock synchronization technique, the clock signal follows slightly after the data transferred across the interface in either direction; col.12, lines 26-29; it is possible to have the memory cell data associated with different row/column addresses latched into the different banks; col.12, lines 10-12*].

As per claim 67, Roy discloses the memory device begins performing the column redundancy check on a first edge of the clock signal and begins performing the internal write operation on another edge of the clock signal [*a transfer made on the rising edge of CLKIN, and a second transfer made on the falling edge (next successive edge) of CLKIN; col.16, lines*

23-27; the column select circuitry using the same clock edge that transfers the first column of the burst, which is the falling edge; col.16, lines 30-33; it is possible to have the memory cell data associated with different row/column addresses latched into the different banks; col.12, lines 10-12].

As per claim 68, Roy discloses another edge comprises the next successive edge of the clock signal after the first edge [*a transfer made on the rising edge of CLKIN, and a second transfer made on the falling edge (next successive edge) of CLKIN*; col.16, lines 23-27].

As per claim 69, Roy discloses the memory device begins the internal write operation in response to a column address trap signal, and the memory device includes a control circuit to assert the column address trap signal synchronously with the edge of the clock signal [*column address information is latched into the column address buffers within the column control logic unit 37*; col.26, lines 5-8; *the internal column select signal can be enabled; at that point there needs to be at least the same number of CLKIN pulse edges as the burst count*; col.35, lines 26-29; *operation initiated and controlled by control signals 85 from the control unit 77 to enable the write data buffer unit 78*; col.15, lines 16-19].

As per claim 70, the rationale in the rejection of claim 48 above is herein incorporated.

As per claim 71, the rationale in the rejection of claim 51 above is herein incorporated.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Roy	6,125,421
Hsu et al.	5,889,727
Roy	5,805,873
Shibata et al.	5,761,139

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 17, 2005



Mardochee Chery
Examiner
AU: 2188



Pierre M. Vital
Primary Examiner
AU 2188